APPLICATION NOTE

17 MAY 2014

JITTERBUG® | AUDIO CLOCK WAVEFORM

JITTER MANAGEMENT, CLOCK RECLAMATION & CHANNEL DUPLICATION

Jitter was introduced when Sony and Philips introduced the CD in 1982. Playback jitter is the inaccuracy in the clock timing of digital data, and it is a pervasive problem with digital audio. As digital audio systems take the stage, issues with jitter become commonplace and problematic.

The purpose of IOL's Jitterbug product is to manage jitter in the digital audio data stream; mitigate cable capacitance and other delay factors by recovering and reclaiming the digital clock embedded in the audio signal.

Below is a representation of the audio waveform seen on 100 feet of 75Ω coax, illustrating the clock variance:

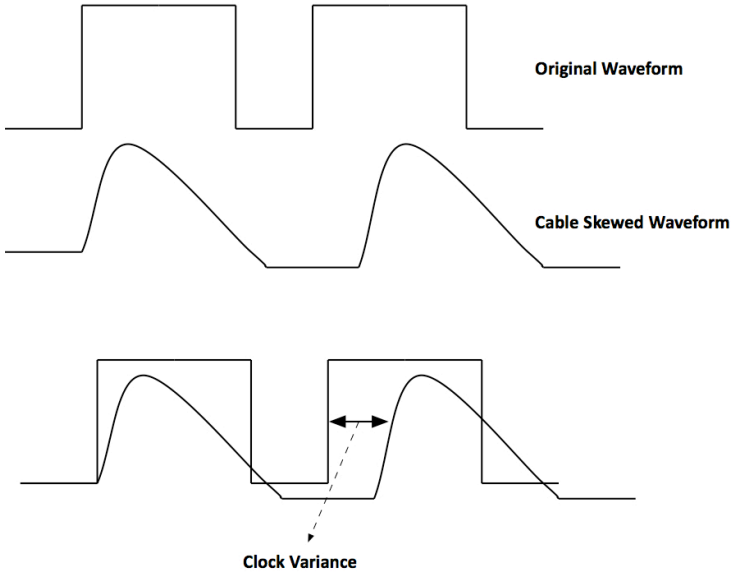

FIG. 1. Clock variance, jitter origination.

Latency in live performances created by interconnect, A/D and D/A conversion processes, console, and front of house DSP, can be as great as 18ms - 24ms, leaving *zero margin* or tolerance for any extra delays in audio signal transport.

Cable capacitance, electromagnetic interference (EMI), and/or crosstalk, create jitter that often overwhelms this *zero margin* state. As the audio clock's waveform travels the length of the cable and approaches the target receiver, this square wave gets rounded off, so that the leading edge gets delayed.

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This creates distortion and may also inject spurious signals such as clicks, pops, etc., into the audio data stream. What was sent is not what gets received.

Below, a screen shot of test results on 100 feet of 110Ω AES shielded twisted 24AWG pair. The green is the originally generated audio waveform. The yellow overlay is the received signal, illustrating what the cable capacitance, velocity of propagation, inductance and other forms of delay, inherent in *every cable*, do to the clock signal:

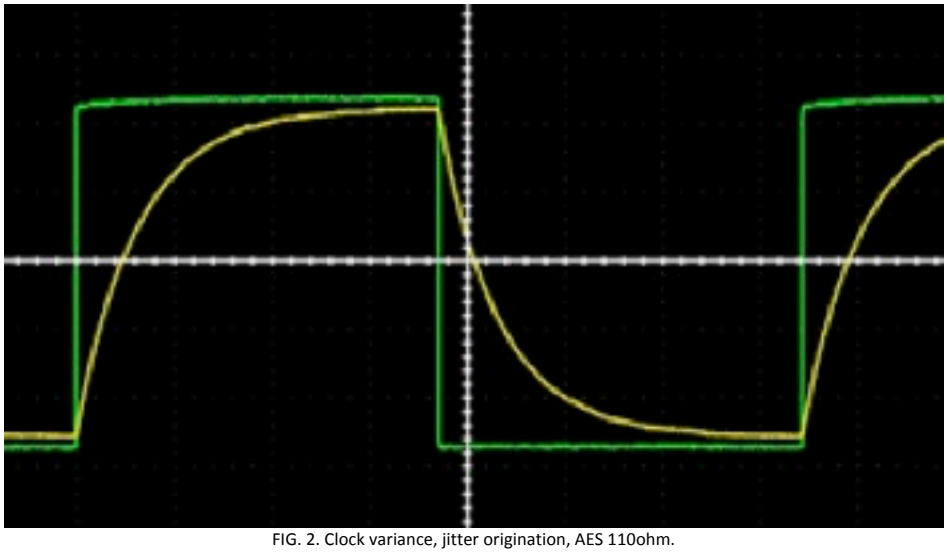

FIG. 2. Clock variance, jitter origination, AES 110ohm.

A long cable run to the stage may still need to be routed hundreds of feet further stage left and stage right. AES bitstreams in such cable lengths will include line-induced jitter; even minimal capacitance in a cable has been shown to inject abundant jitter into the digital audio data stream. A longer cable run creates more delay. Cables skew digital audio signals primarily by attenuating the highest frequencies.

Many factors impact the quality of the digital audio signal cable transmission. All cables, even the highest quality, are subject to their changing environments. EMI/RFI ingress and egress affects all cable assemblies and most connectors.

Other influences impact the quality of the digital transmission. A particular venue's infrastructure and environment. Abused equipment. Old cables that have been twisted and flexed repeatedly. Low-cost or legacy equipment not featuring high performance DAC's and filters. A nearly endless list.

As a digital signal travels down a cable and across numerous mating connectors of dubious quality, typically built in low-cost manufacturing zones by the lowest bidder, the cumulative capacitance, resistance, velocity of propagation, EMI, and inductance of these elements degrade and alter the shape of the transmitted square waveform.

As shown above, this manifests itself in a rounding off of the rise and fall times, as well as making the amplitude of the wave smaller, all of which creates significant difficulty for the receiving device to reliably detect the original data. Excessive jitter can prevent the signal from being resolved at all.

Since jitter is dissonant distortion, it will be more audible than harmonic distortion. Embedded clocks, such as clocking over ADAT or AES, typically suffer more jitter than word clocks. In order to properly manage and mitigate jitter to deliver a crisp, clean audio signal, clock recovery is needed.

Jitterbug manages jitter by reducing it to inaudible levels through clock waveform reclamation. Jitterbug also boosts the digital signal, enabling further transmission distances. Outputs can be configured to either mirror or duplicate outbound channels.

Correcting even the best cable's faults delivers the highest quality digital audio signal.

SIMPLIFIED BLOCK DIAGRAM

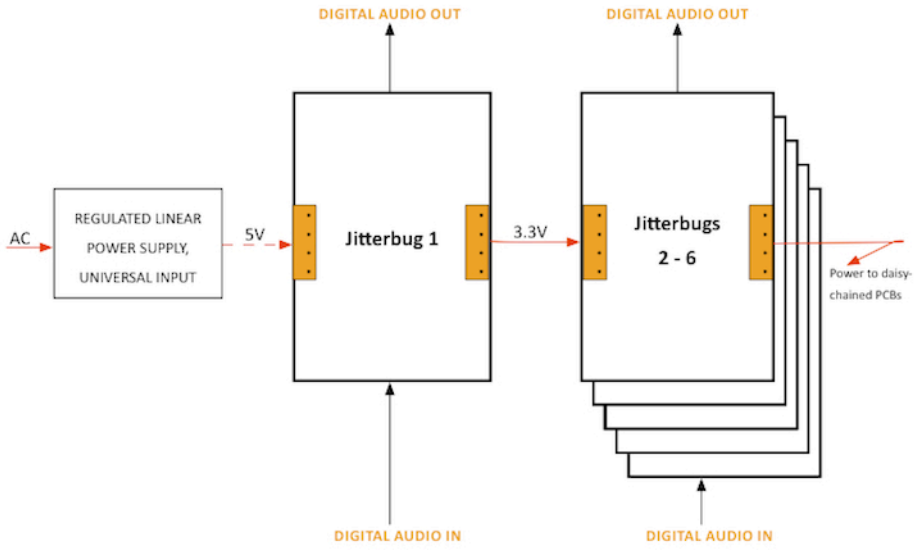

FIG. 3. Jitterbug Simplified Block Diagram.

DESIGN DETAILS

Jitterbug® supports AES3, IEC60958, S/PDIF & EIAJ CP1201 interface standards. Jitterbug directly accepts a cable run of AES digital audio, reclocks the audio data stream mitigating jitter and boosts the signal.

Outbound audio is biphase-encoded and driven back on to the cable.

Each Jitterbug board features 4 channels of AES digital audio. Six boards can be daisy-chained together using the onboard connectors to create a 24 channel system (Mirror mode), fitting into a 1U enclosure.

Jitterbug operates in two distinct, jumper-selectable IO modes:

- Mirror mode (default), where Ch1 IN is routed to Ch1 OUT (4ch IN/4ch OUT);
- Dup mode, where Ch1 IN is duplicated on Ch1 & Ch2 OUT, and Ch3 IN is duplicated on Ch3 & Ch4 OUT (2ch IN/4ch OUT).

In Mirror mode, a 12/12ch system requires 3 PCBs; in Dup mode, a 12/24ch system requires 6 PCBs.

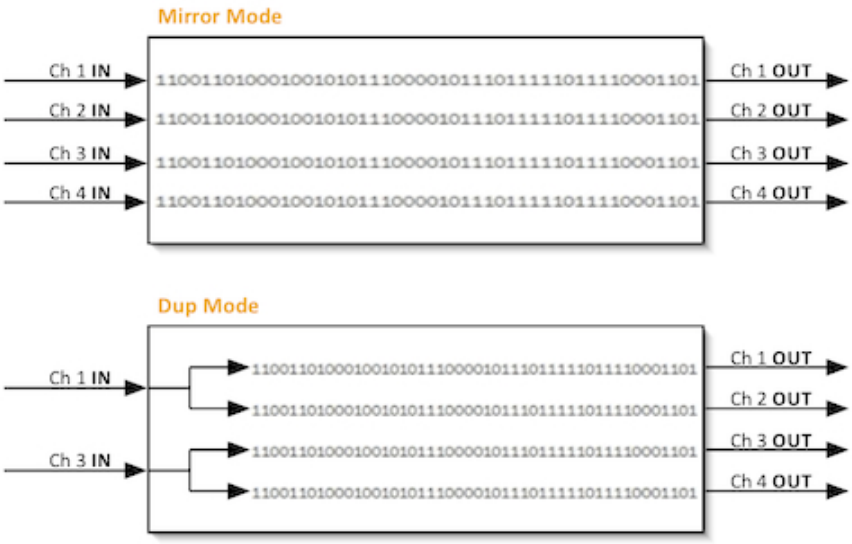

FIG. 4. Jitterbug's multi-mode operation options. Digital audio stream represented by 1's & 0's. All functional settings labeled in PCB artwork.

Jitterbug's Dup mode functionality means that the board can also be packaged as a reliable, high-quality channel duplicator. This stand-alone product would replicate and boost each channel's signal for re-routing in new and existing wiring installations and applications as diverse as broadcasting, studio, theatre, stadiums, houses of worship and conference centers.

Because the board supports both AES and S/PDIF audio, a high-end consumer audio product could also be offered.

Selectable audio inputs and outputs include 100ohm AES twisted pair or 75ohm coax. These impedance's could also be mixed, if necessary; e.g., 75ohm IN, 110ohm OUT.

The system supports audio up to 192kHz, 24bits, and features frequency sampling detection at 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz & 192kHz.

Each channel's receiver meets the AES3 specified minimum 200mV peak-to-peak input level for a clock recovery circuit.

Each channel's transmitter provides an RS-422 output, which meets the AES3 requirements for a balanced line driver.

PRODUCT KIT

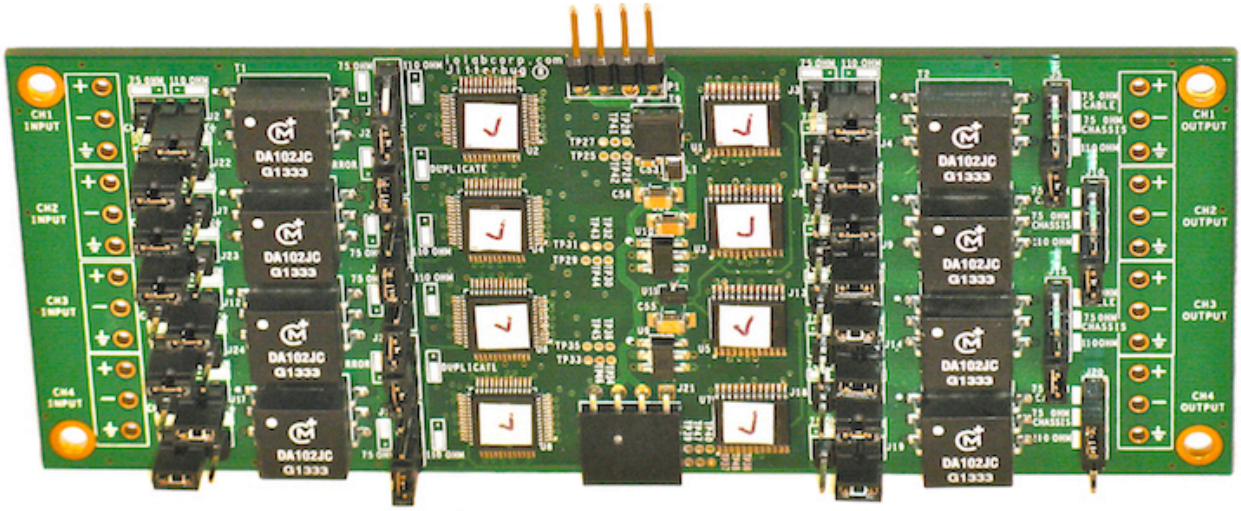

FIG. 5. Jitterbug prototype with jumper selections: 110ohm I/O; chassis ground; Mirror mode. All functional settings labeled in PCB artwork.

The Jitterbug Product Kit includes:

- Documentation on the specified, commercially available linear power supply;
- Jitterbug PCBs required;
- Final assembly instructions;
- Test notes.

Instructions are basic: the power supply gets wired to Jitterbug #1, and then subsequent Jitterbugs are simply plugged into one another. The incoming and outgoing cables can be soldered directly to the boards or to an intermediary interface such as an XLR, D-Sub, RCA or Multipin. The product can be mounted in a standard 1U enclosure or in vented custom metal.

IOL's Assembly Partners private-label Jitterbug embedded enclosures with their logo and brand identifications. Contact us for a customized, web site ready description on the product's functionality and features.

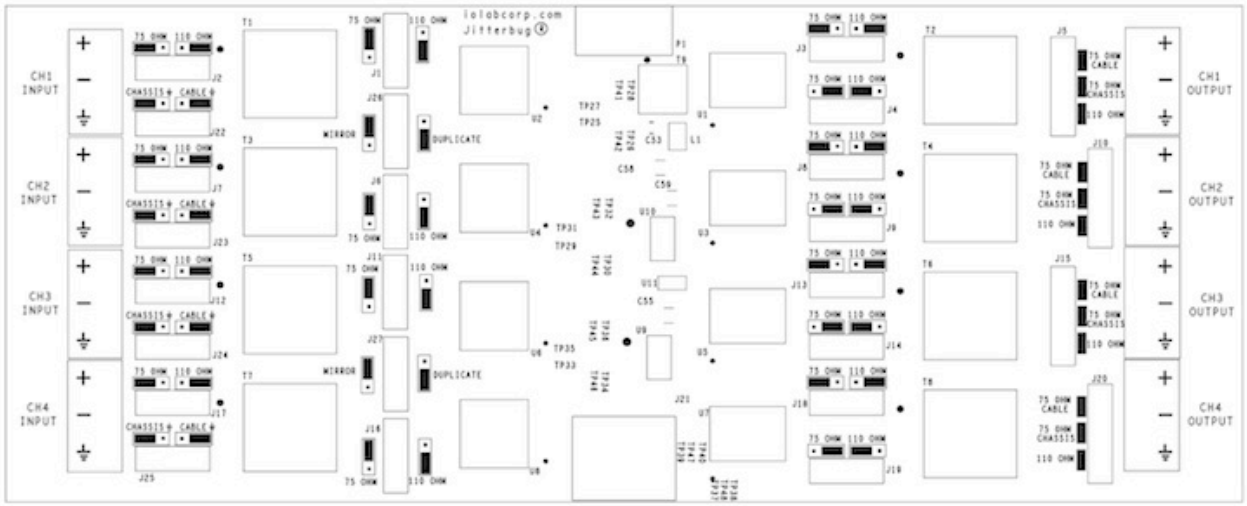

FIG. 6. Jitterbug PCB top silkscreen. All functional settings labeled in PCB artwork.