07 July 2014

JITTERBUG v1.0 RELEASE & ERRATA NOTES

1. PCB trace issues have created mislabeled connectors at J4, J9, J14, and J19.

The 75 Ohm and 110 Ohm jumper positions are swapped.

As long as the jumper is set correctly, this does not affect the performance of the board.

These traces will be fixed in an upcoming release.

2. Power to be applied to Jitterbug at incoming power connector P1 from specified CUI supply:

Pins 1 & 4 = Ground
Pins 2 & 3 = +5V

Pin 1 on Jitterbug's power input is identified by a square solder post (underneath the board).

After supplying power to the first Jitterbug in a chain, the boards will pass/route all power to any downstream domains (maximum 6 Jitterbugs tested).

3. Since we were focusing exclusively on AES digital audio, SPDIF is non-functional in this version. However, only a few minor design/component changes are required to activate this feature.

4. Testing has been completed. We have verified that Jitterbug does a great job of AES audio clock reclamation, as well as discovering how badly 100 – 300 feet of cable distorts the digital audio waveform.

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